

On Verifiable Delay Functions from Time-Lock Puzzles

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(Trapdoor) Verifiable Delay Functions [BBBF18]

A function $F : \mathcal{X} \rightarrow \mathcal{Y}$ that is **slow to compute** (without trapdoor) but **fast to publicly verify**.

- $\text{Setup}(\lambda, t) \rightarrow (\text{pp}, \text{td})$ public params + trapdoor
- $\text{Eval}(\text{pp}, x) \rightarrow (y := F(x), \pi)$ sequential time t
- $\text{TEval}(\text{td}, x) \rightarrow (y, \pi)$ trapdoor eval, time $\text{polylog}(t)$
- $\text{Ver}(\text{pp}, x, y, \pi) \rightarrow \{0, 1\}$ time $\text{polylog}(t)$

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Constructions: (iterated) **sequential function** + **succinct proof system** [Pie19, Wes19, BBBF18, FPS22]

Time-Lock Puzzles [RSW96]

A puzzle that is fast to generate but slow to solve. quick (randomized) generation of preimages.

- $\text{PGen}(\lambda, t, s) \rightarrow z$

randomized, time $\text{polylog}(t)$

- $\text{Sol}(z) \rightarrow s$

sequential time t

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Indistinguishability of puzzles (sequentiality):

for any s_0, s_1 , $\text{PGen}(t, s_0) \approx_{\text{depth} \ll t} \text{PGen}(t, s_1)$.

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Constructions:

- [RSW96]: repeated squaring in hidden-order groups
- [BGJ⁺16]: worst-case non-parallelizing languages (wcNPL) + randomized encodings

VDFs vs. TLPs: two ends of the same axis

	VDF	TLP
generate / setup	$\text{polylog}(t)$	$\text{polylog}(t)$
“hard” direction	evaluate in t	solve in t
verify	$\text{polylog}(t)$	— (verifier has s)
reusable?	yes	no (one-time)
preprocessing?	yes	no

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Can we build a (publicly verifiable) VDF *from* a TLP?

Our result

Main theorem

(one-time) VDF from TLP + iO + (injective) OWF.

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Corollary (with [BGJ⁺16, BPW16])

(one-time) VDF from $\text{wcNPL} + \text{(polynomially-secure) iO} + \text{OWF}$.

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Our VDF is the first to:

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Caveat: sequentiality holds only *without* preprocessing (i.e., one-time) $\implies$ fresh pp per evaluation.

Step 1: a delay function from TLP + iO

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$\text{Sample}_{[t, k_1, k_2]}(x)$

$s := \text{PPRF.FEval}(k_1, t \parallel x)$ pseudorandom solution

$z := \text{TLP.PGen}(s, t; \text{PPRF.FEval}(k_2, t \parallel x))$ derandomized puzzle

return z

$\text{pp} := \text{iO}(\text{Sample})$, with t, k_1, k_2 hard-wired.

To evaluate: run Sample to get z , then $s := \text{TLP.Sol}(z)$; output s .

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Perfect TLP correctness $\implies$ unique solution s .

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Problem: A SNARG would give only selective / computational soundness (or needs subexponentially-secure iO [WW24, WZ24]).

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- Wrong $s^* \neq s$ accepting $\implies f(s^*) = f(s)$, contradicting injectivity. **Perfect soundness.**
- **Trapdoor** $\text{td} := k_1$: $\text{TEval}(\text{td}, x) = \text{PPRF.FEval}(k_1, t \parallel x)$ (no solving needed).

Sequentiality: proof via punctured programming [SW14]

Goal: reduce sequentiality of the VDF to sequentiality of the TLP.

- Sequentiality game: a **depth-bounded** adversary gets pp and a random challenge x^* , and needs to output y^* such that $y^* := \text{Eval}(pp, x^*)$.

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- Sequentiality game: a **depth-bounded** adversary gets pp and a random challenge x^* , and needs to output y^* such that $y^* := \text{Eval}(pp, x^*)$.
- **Key observation:** the reduction may *pre-sample* x^* together with pp .
- Hardwire the challenge puzzle z^* and proof π^* into the obfuscated circuit.

Sequentiality: the hybrids on the x^* branch

$pp := \text{iO}(\text{Sample}), \text{challenge } x^*$

precompute using original keys k_1, k_2 :

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$\pi^* := f(s^*)$

$\text{Sample}(x)$:

if $x = x^*$ then return (z^*, π^*)

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adversary wins iff it outputs s^*

Hybrids:

- H_0 : real experiment

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now $z^* \equiv$ honest TLP puzzle

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- H_5 : puzzle from s_2^* , win on s_1^*
invoke **TLP sequentiality**

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- H_5 : puzzle from s_2^* , win on s_1^*
invoke **TLP sequentiality**
- proof leaks only $f(s_1^*) \implies$
one-wayness of f ✓

Why only “one-time”?

- The reduction **hardwires the challenge puzzle z^* into pp** .
- A *preprocessing* adversary receives pp (the obfuscated circuit containing z^*) and may run **unbounded sequential** computation on it *before* the clock starts.
- But TLP sequentiality only holds against depth-bounded adversaries. **Reduction breaks.**

Extensions

Efficient-verifier VDF: the circuit also outputs a **signature** σ

$$\text{Sample}_{[t, k_1, k_2, \text{sk}]}(x)$$
$$s := \text{PPRF.FEval}(k_1, t \parallel x)$$
$$z := \text{TLP.PGen}(s, t; \text{PPRF.FEval}(k_2, t \parallel x))$$
$$\pi := f(s); \sigma := \text{Sig.Sign}(\text{sk}, x \parallel \pi \parallel z)$$
$$\text{return } (z, \pi, \sigma)$$

Ver: accept iff $f(s) = \pi$ and $\text{Sig.Ver}(\text{pk}, \sigma, x \parallel \pi \parallel z) = 1$ (no re-running obfuscated circuit!).

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Richer trapdoors: trapdoor evaluation *is* a PRF evaluation $\implies$ richer PRFs give richer VDFs:

- Trapdoor-homomorphic VDFs: key-homomorphic (constrained) PRF [BFP⁺15, BV15]
- Trapdoor-constrained VDFs: constrained PRF [BW13]

The bigger picture: relating VDFs and TLPs

Known *generic* relations between the two timed primitives:

$\text{TLP} + \text{iO} + (\text{injective}) \text{OWF} \implies \text{one-time VDF}$ this work

$\text{trapdoor VDF} \implies \text{TLP: } z := (\text{pp}, x, s \oplus y)$ folklore

where $(\text{pp}, \text{td}) \leftarrow \text{VDF.Setup}$, $(y, \pi) \leftarrow \text{VDF.TEval}(\text{td}, x)$

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... and these detours are *inherent* [AAA⁺26]:

No *fully black-box* construction of VDF from TLP.

Conclusion

A new design paradigm: $\text{TLP} + \text{iO} + \text{OWF} \implies (\text{one-time}) \text{VDF}$.

- Perfect soundness, pseudorandom outputs, generic trapdoor VDF.
- Homomorphic/constrained trapdoors.

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Thank you!



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